V. SUBSTITUTE SUMMARY OF THE CLAIMED SUBJECT MATTER

In one embodiment of the invention, independent Claim 1 requires and positively recites, a method for testing (Title, Abstract, Fig 8 & 9a-d) a radio frequency (RF) circuit (Title, Abstract, Fig 2 & 3 & 6) comprising:

observing a signal (PHE or phi_E[k] signal in Figs 2 ([0031] lines 1-2) , 3 ([0034] lines3-6), 6; PHE or "filtered PHE" in Fig 10 ([0059], lines 3-6); step "observe internal digital signal" 805 in Fig 8 ([0048] lines 1-4); steps 902, 922, 942, 962 in Figs 9a-d) from the RF circuit (in Fig 10: PHE signal fed into signal analyzer 1005), wherein the signal is a digital signal from within a processing portion of the RF circuit, wherein the signal has a high degree of correlation with an RF output of the RF circuit, and wherein the observing occurs outside of the RF circuit;

manipulating the signal outside of the RF circuit (in Fig 10: PHE internal signal fed into signal analyzer 1005, which is external to the RF circuit); and

producing a metric (output of signal analyzer 1005 in Fig 10) for the test outside of the RF circuit based on results from the manipulating.

In another embodiment of the invention, independent Claim 25 requires and positively recites, a method for testing (Title, Abstract, Fig 8 & 9a-d) a radio frequency (RF) circuit (Title, Abstract, Fig 2 & 3 & 6) containing an all-digital phase-locked loop comprising:

setting the all-digital phase-locked loop to a certain bandwidth ([0048] line 12; [0055] lines 9-11);

observing a signal (PHE or phi_E[k] signal in Figs 2 ([0031] lines 1-2) , 3 ([0034] lines3-6), 6; PHE or "filtered PHE" in Fig 10 ([0059], lines 3-6); step "observe internal digital signal" 805 in Fig 8 ([0048] lines 1-4); steps 902, 922, 942, 962 in Figs 9a-d) from the RF circuit (in Fig 10: PHE signal fed into signal analyzer 1005), wherein the signal is a digital signal from within a processing portion of the RF circuit, wherein the signal has a high degree of correlation with an RF output of the RF circuit, and wherein

the observing occurs outside of the RF circuit;

manipulating the signal outside of the RF circuit (in Fig 10: PHE internal signal fed into signal analyzer 1005, which is external to the RF circuit); and

producing a metric (output of signal analyzer 1005 in Fig 10) for the test outside of the RF circuit based on results from the manipulating, wherein the test is for estimating phase noise power ([0054] lines 1-10; [0055] lines 12-15) and the signal is an output of a phase detector ([0059] lines 1-6), and wherein the manipulating comprises calculating a mean square error of the signal ([0055] lines 9-11).

In yet another embodiment of the invention, independent Claim 32 requires and positively recites, a circuit comprising:

a processor ([0059] lines1-3; signal analyzer 1005 in Fig 10) coupled to a radio frequency (RF) circuit ([0058] lines 1-11ADPLL 200, 300, 600 of Figs 2, 3, 6, respectively), the processor containing circuitry to manipulate digital signals (PHE or "filtered PHE" in Fig 10, "other signals" in [0061]) from the RF circuit to provide a performance metric (output of signal analyzer 1005) for the RF circuit; and

a control signal input ([0059], lines 9-10; "control", "window" inputs to signal analyzer 1005) coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals.

In still yet another embodiment of the invention, independent Claim 41 requires and positively recites, a circuit comprising:

a reference phase accumulator ([0031] lines 3-6; 205 in Figs 2 & 3) coupled to a signal input (FREF), the reference phase accumulator containing circuitry to compute a reference phase ([0031] line 6; R_R[k] output of 205);

a phase detector ([0031] lines 2-3; 210) coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference ([0031] lines 1-2; phi_E[k] output of 210) between the reference phase and a variable phase;

a digitally-controlled oscillator ([0033] line 7; 225) coupled to the phase detector,

wherein the performance of the DCO can be ascertained by a test circuit (signal analyzer 1005) outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation; and

a variable phase accumulator ([0032] lines 1-4; 235; Figs 2 & 3) coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase.

In yet still another embodiment of the invention, independent Claim 44 requires and positively recites, a circuit comprising:

a reference phase accumulator ([0031] lines 3-6; 205 in Figs 2 & 3) coupled to a signal input (FREF), the reference phase accumulator containing circuitry to compute a reference phase ([0031] line 6; R_R[k] output of 205);

a phase detector ([0031] lines 2-3; 210) coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference ([0031] lines 1-2; phi_E[k] output of 210) between the reference phase and a variable phase;

a digitally-controlled oscillator ([0033] line 7; 225) coupled to the phase detector, wherein the performance of the DCO can be ascertained by a test circuit (signal analyzer 1005) outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation;

a variable phase accumulator ([0032] lines 1-4; 235; Figs 2 & 3) coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase; and

a loop filter coupled to the phase detector and the DCO ([0033] lines 1-4 ; [0040] lines 1-6), the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase, wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof ([0033] lines 1-4).

In yet a further embodiment of the invention, independent Claim 48 requires and positively recites, a method for operating a cellular phone ([0044] lines 6-7, "if the device under test is a cellular telephone"), comprising:

performing ([0044] lines 5-8, "carrier can run tests on the device") built-in self-test (BIST) on a parameter associated with the cellular phone; and

reporting ([0044] lines 8-9, "and then the device can provide the results to the carrier") to a cellular service provider through a wireless medium when the BIST reports the parameter to be degraded beyond a limit.